Testing Integral and Differential Non-Linearity of ADC Using Servo Loop Solution

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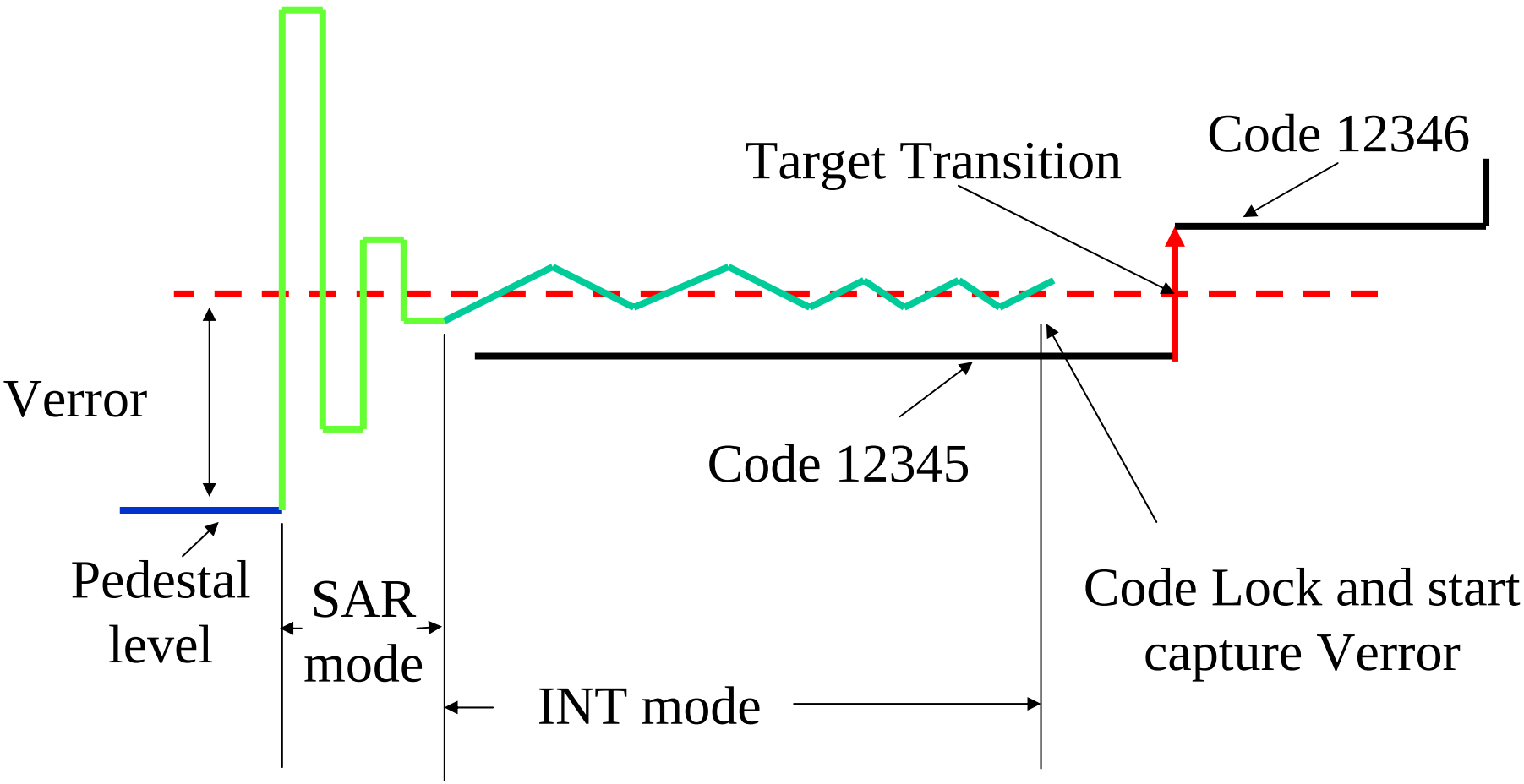
Overview

- **Solution for INL/DNL testing of high-resolution Analog-to-Digital converter (ADC)**
- **Supported device types**
  - **20-bit parallel**
  - **32-bit serial max.**
- **Single-ended and differential input signals**
- **Supports multiple data formats**
  - **1's Complement, 2's Complement, Inverted etc.**
- **Designed for multi-site testing capability**
  - **Dedicated Servo Loop Module per DUT**
  - **Shared DC Reference Module**

Servo Loop Operation



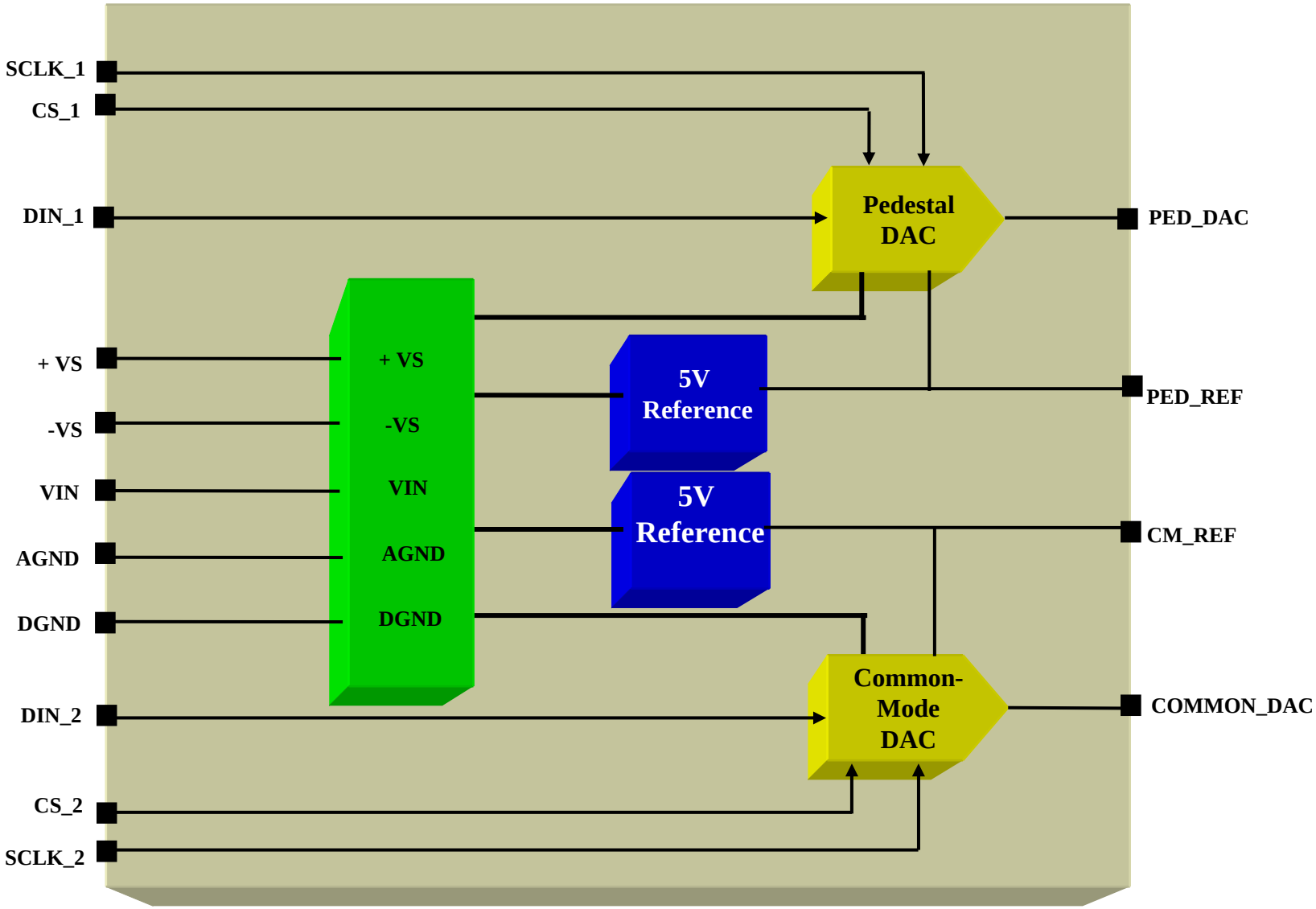
Target Level = Pedestal level + Verror

DC Reference Module:

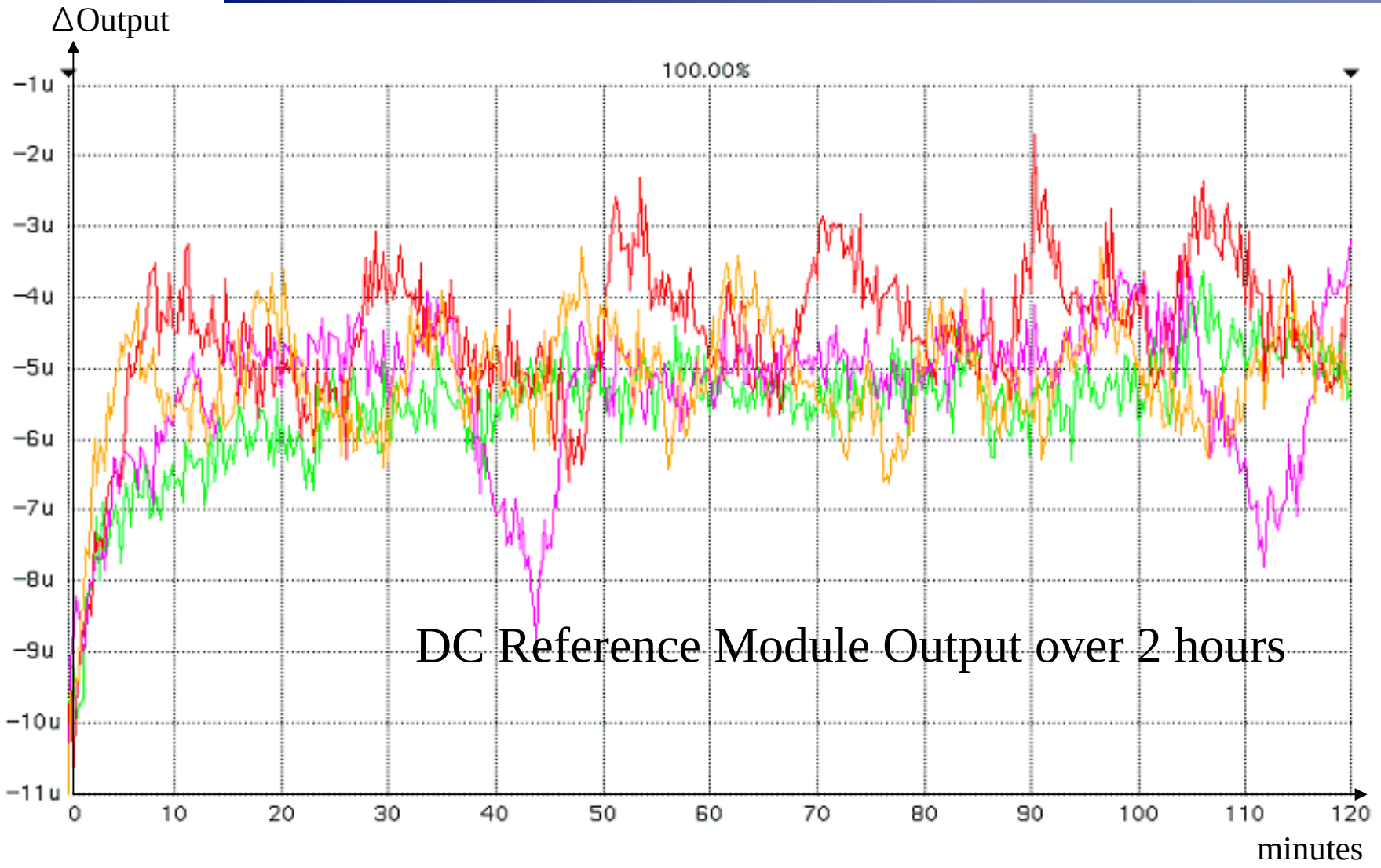
The DC Reference Module provides

- **Pedestal Voltage near target code transition level**
- **Common-Mode voltage for differential signal**
- **Max +/- 12.5V driving capability**

DC Reference Module



DC Reference Stability



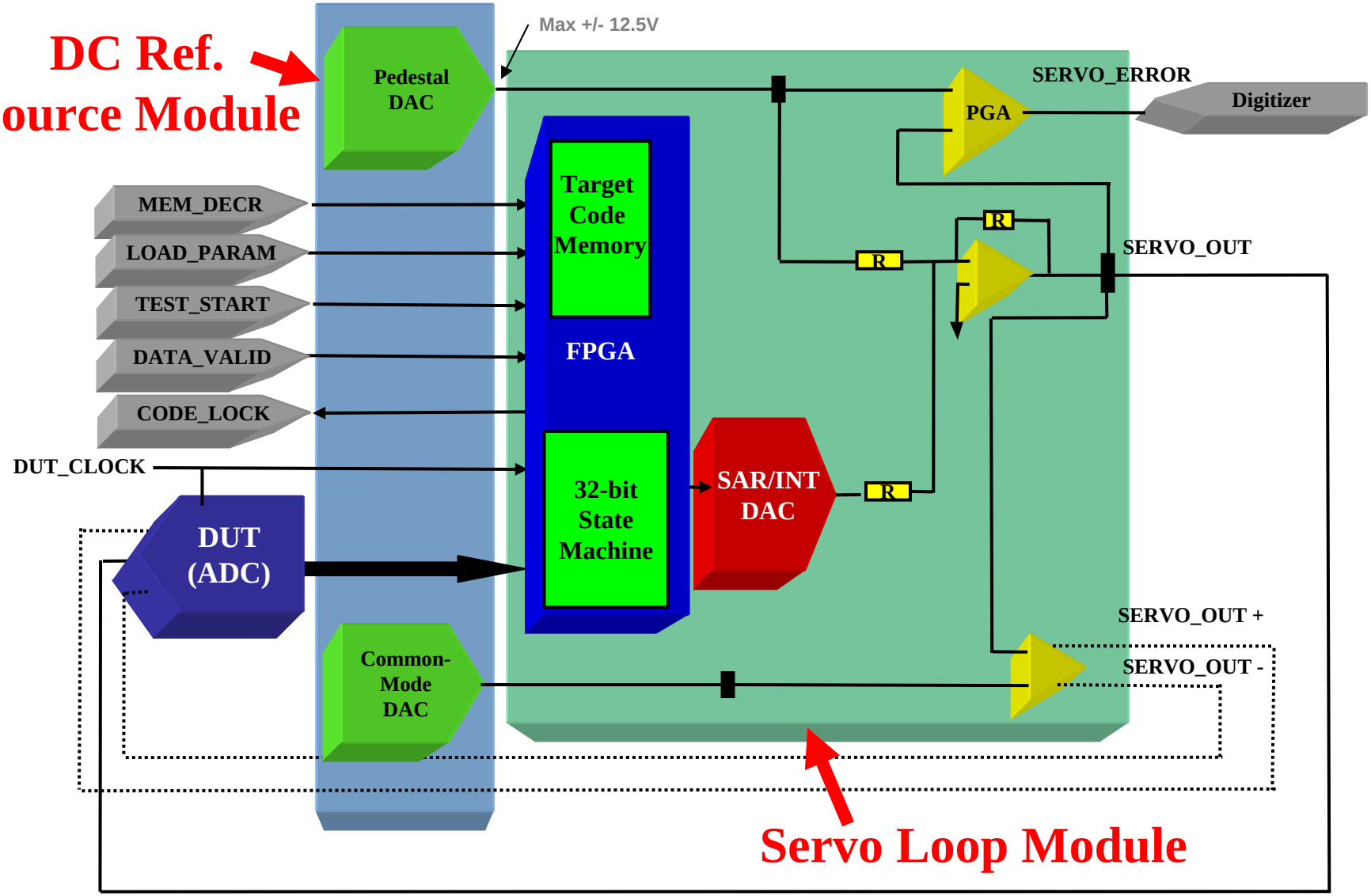
Servo Loop Module:

- **The Servo Loop's makes the main decisions**
  - **Updates the input to the ADC based upon the current output.**
  - **Asserts "Code Lock" after the code has been successfully found.**
- **Driving error voltage between Pedestal level and SAR DAC through gain amplifier**

Servo Features

- **Ability to amplify error voltage and measure it to calculate the transition voltage for the code**
  - **Gain of 1, 10, 100, 1000**
- **Programmable SAR cycles (max. 14)**
  - **For initial binary search of transition edge**
- **Adjustable servo range**
  - **+/- (Reference Voltage / 10)**
  - **Ref. voltage 1 to 5V**
- **Programmable integrator step size (max. 15 steps)**
  - **Ability to control servo step size during integration**
- **Ability to “lock on” rising or falling edge**

Servo Loop & Ref Source



Programming-Software Calibration

- **Three calibration factors need to be measured for each code**
  - **Pedestal Voltage / Common-Mode Voltage**
  - **Composite Offset Error**
  - **Composite Gain Error**

- **The calibration data is stored in a global structure object and written to a file that is later read and accessed when required by the test program.**

Calculating code edge voltage

Code transition voltage is calculated from the measured ERROR_OUT voltage and calibration factors as follows.

code transition voltage =

pedestal voltage +

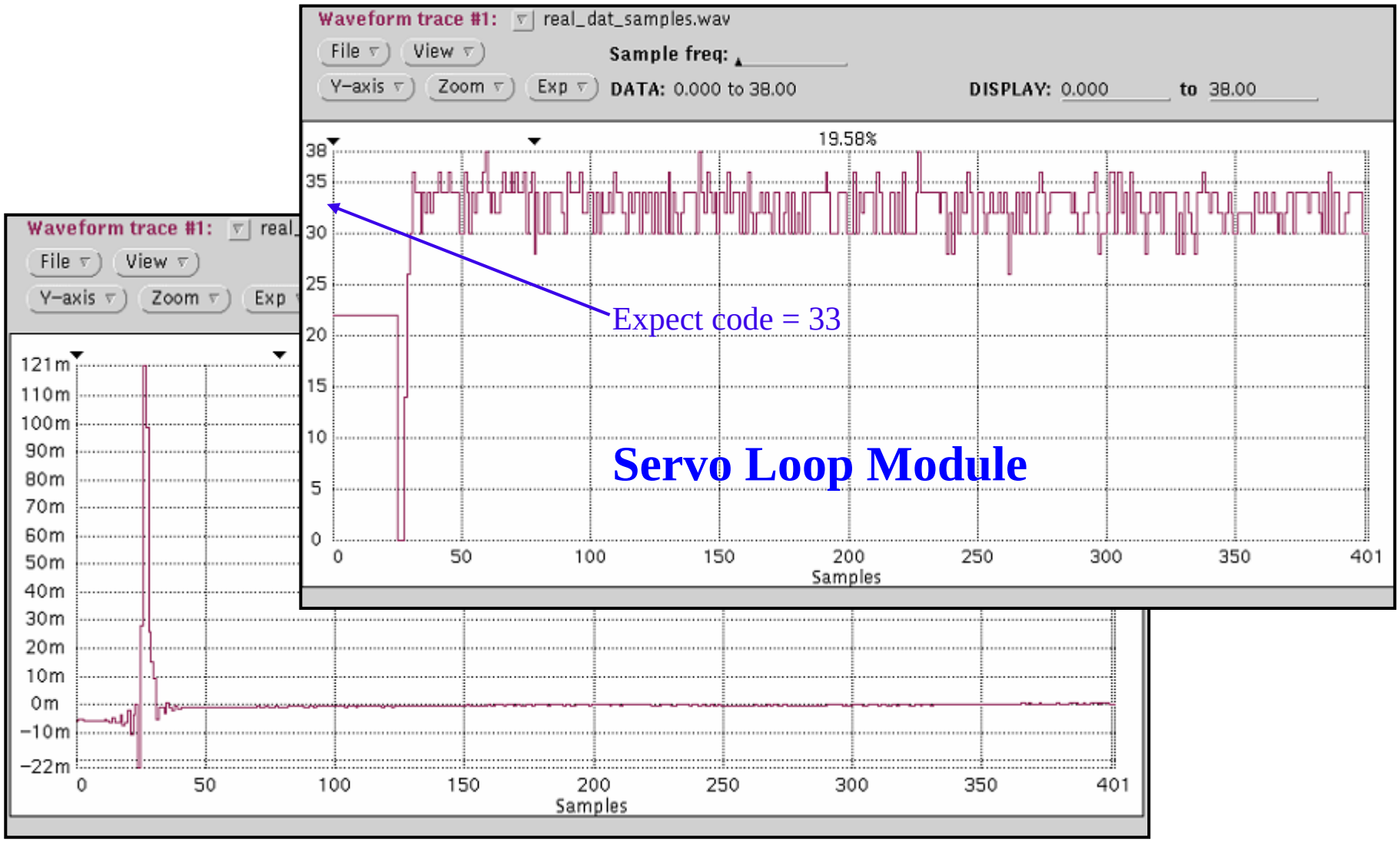
[(averaged error voltage - offset error) /

{servo error amplifier gain * (1 + gain error)}]

Test Time Reduction

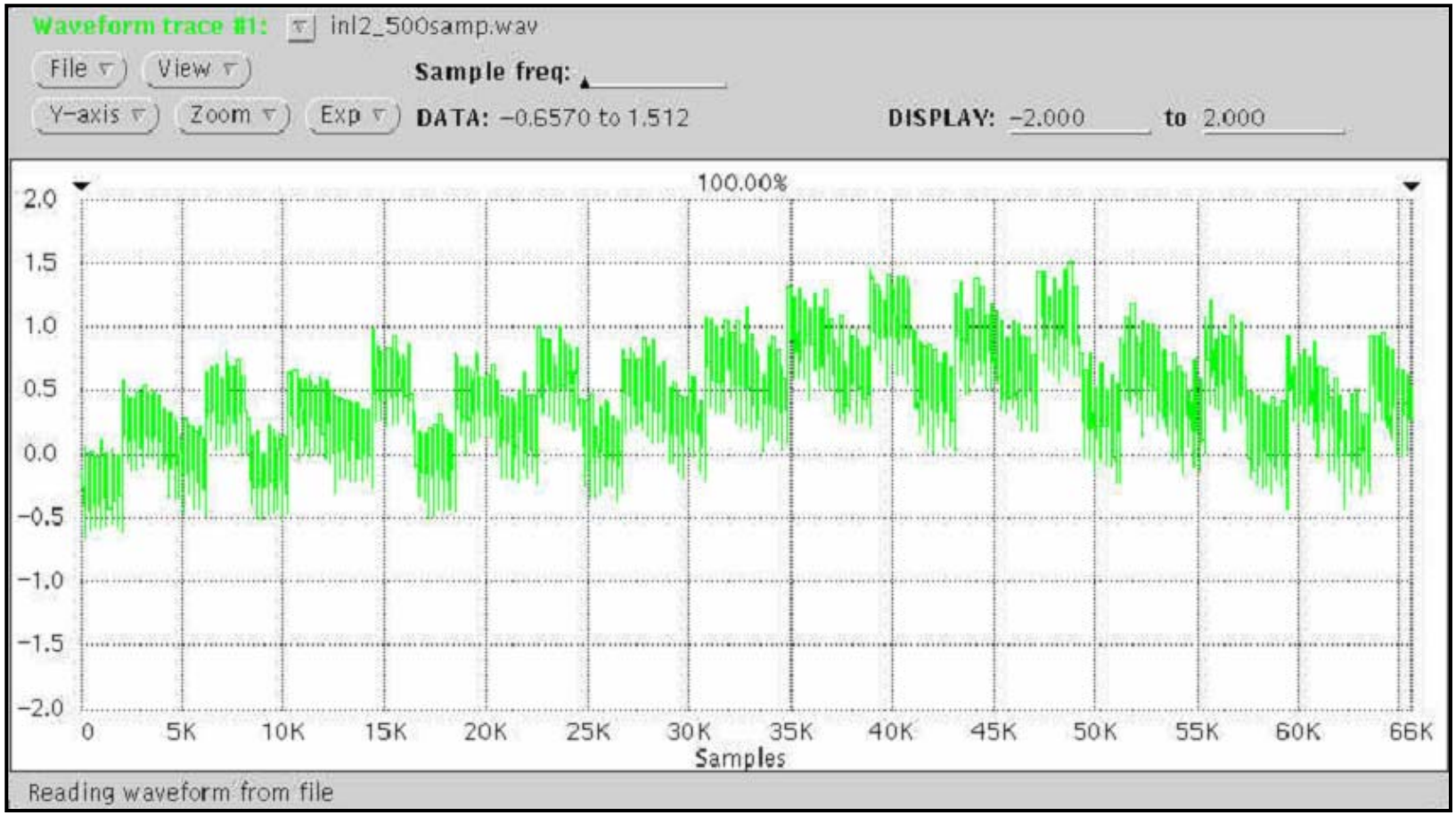
- **Test time reduced by testing a reduced code set**
  - **For example, for a 16-bit application 2000 codes are tested out of a possible 65535 codes**
- **For a 16-bit application test time was reduced to 12 seconds vs. 22 seconds using Ramp INL/DNL**
- **Multi-site test**

Typical Performance

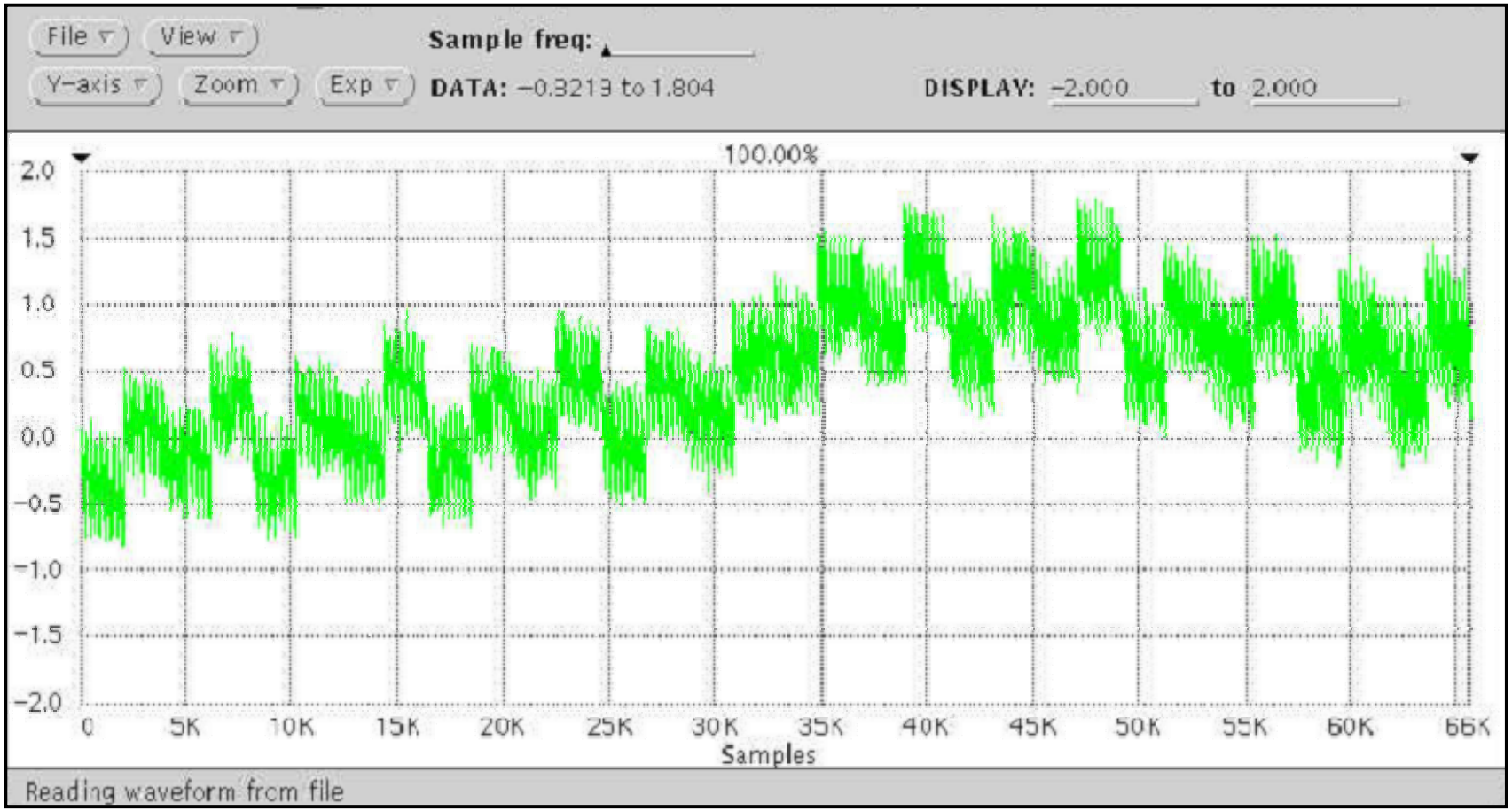


Linearity Results using Servo Loop Technique
vs.
Ramp Histogram Method

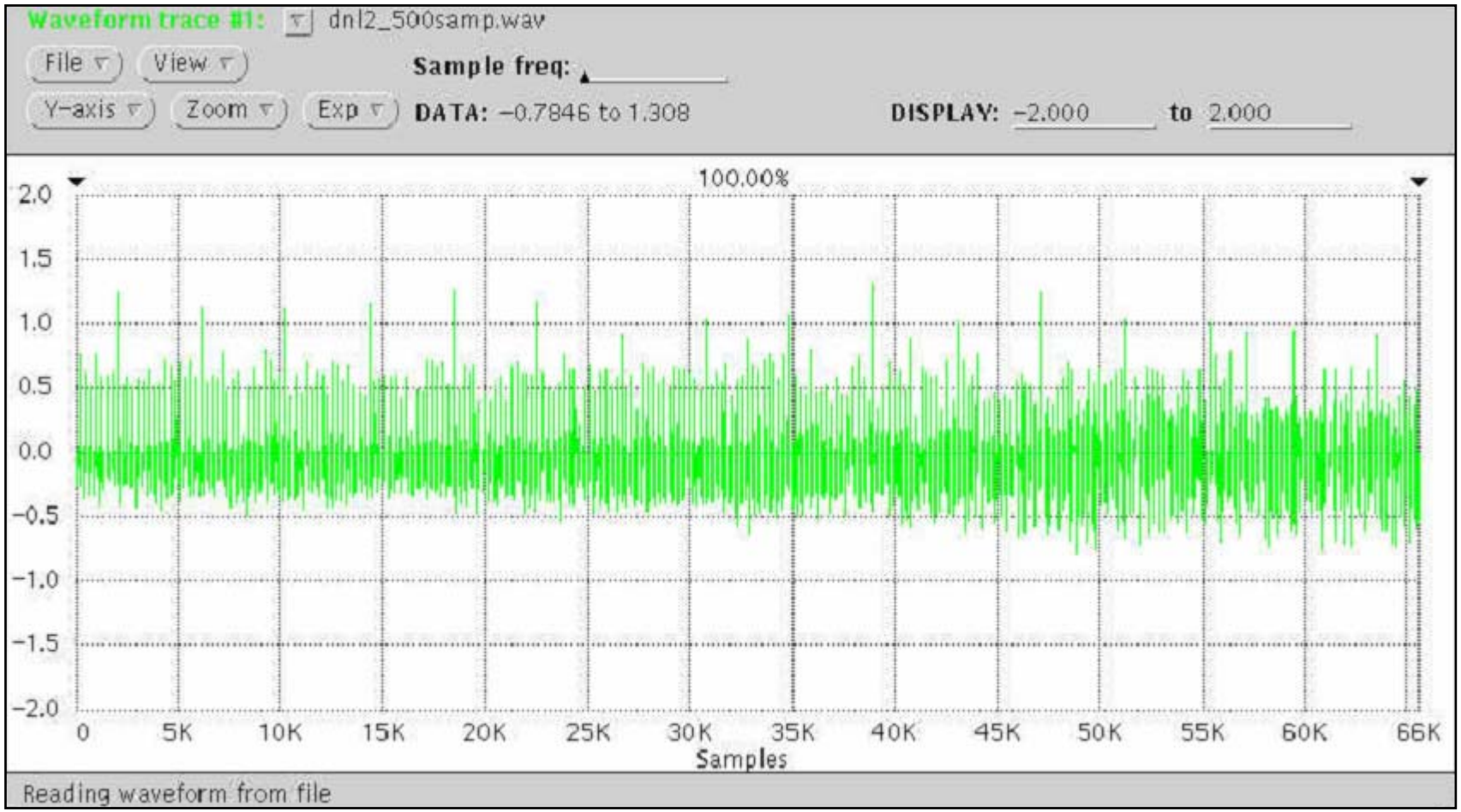
Servo Loop INL



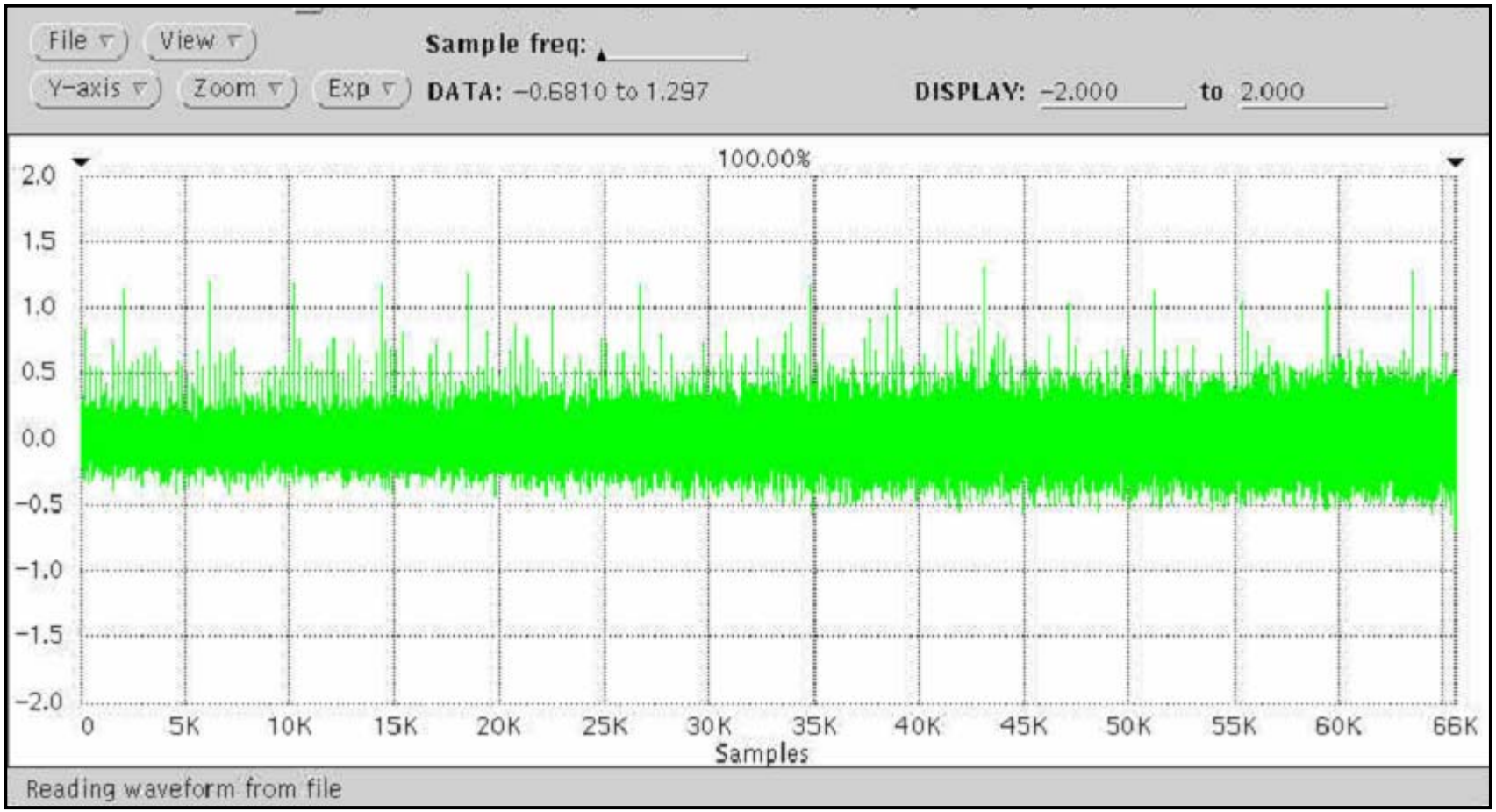
Ramp Histogram INL



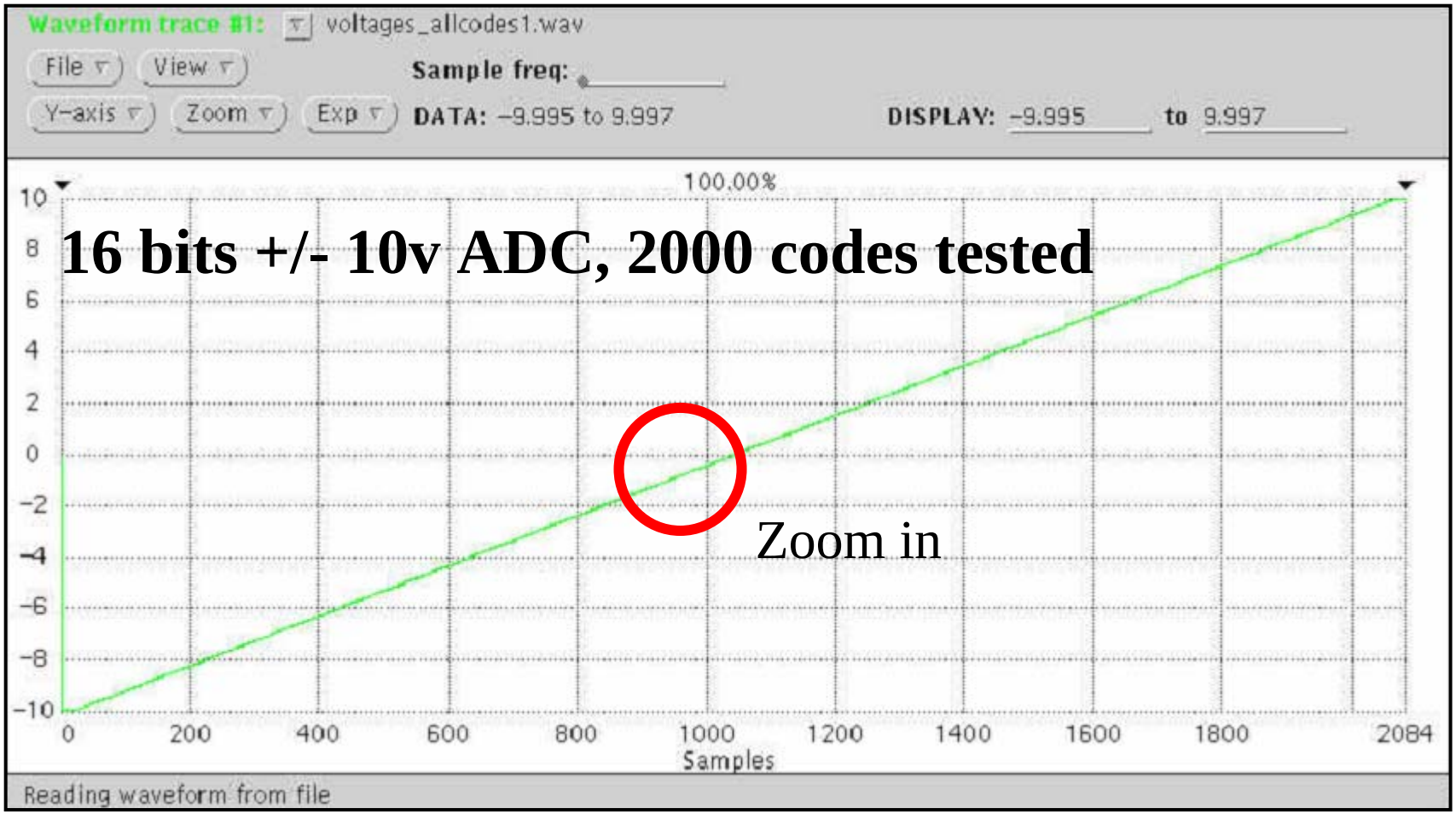
Servo Loop DNL



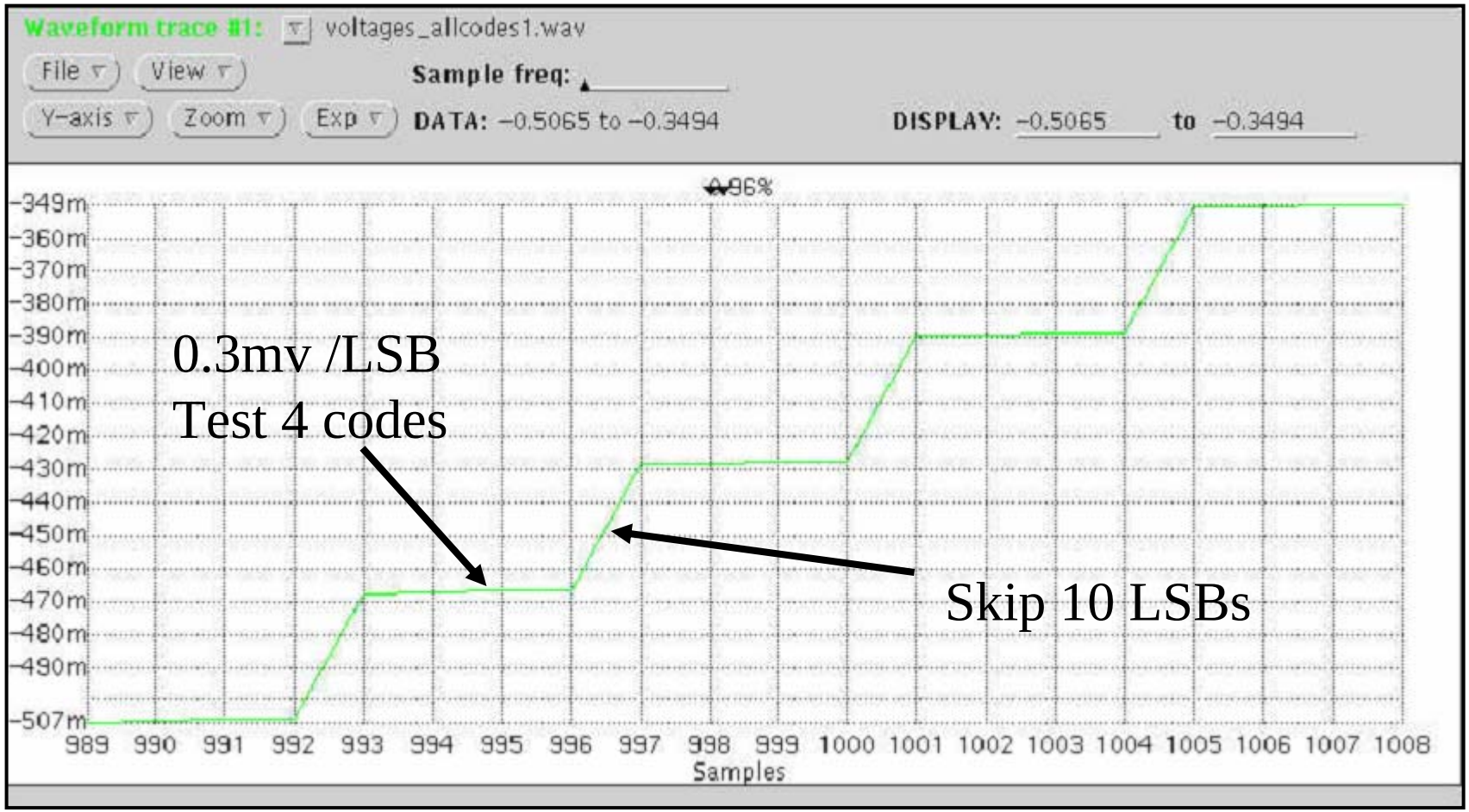
Ramp Histogram DNL



Code Edge Voltages



Code Edge Voltages (Zoomed)



Application DIB